Electronic Version
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# Claims

[c1] A method of forming an NFET having a strained silicon transistor body in a layer of strained silicon, having a strained silicon layer thickness, disposed on a support layer of SiGe alloy, comprising the steps of:
forming a gate dielectric over said strained silicon transistor body;
forming a gate electrode over said gate dielectric;
forming a pair of temporary dielectric spacers on opposite sides of said gate electrode;
removing said strained silicon outside said transistor body and below said pair of temporary spacers by a substantially non-directional process, leaving a buffer portion of strained silicon in said strained silicon layer and outside said transistor body and a first S/D aperture outside said buffer portion;
forming an electrode layer of silicon in said first S/D aperture, making mechanical and electrical contact with said transistor body and with a portion of said support layer of SiGe below said first S/D aperture;
forming transition doped areas between said transistor body and electrode areas in said electrode layer on opposite sides of said transistor body; and

forming transistor electrodes in said electrode areas.

[c2] A method according to claim 1, further comprising a step of:
removing said pair of temporary dielectric spacers after said step of forming said electrode layer of silicon in said first aperture; and
forming said transition doped areas by implanting dopants in said electrode layer of silicon.

[c3] A method according to claim 2, further comprising a step of:
removing SiGe alloy from said support layer below said S/D aperture, thereby extending said first S/D aperture vertically downward to form a second S/D aperture; and forming said electrode layer of silicon in said second aperture with an electrode layer thickness greater than said strained silicon layer thickness.

[c4] A method according to claim 1, in which said temporary spacers have a thickness abutting said strained silicon layer such that said buffer portion of strained silicon in said strained silicon layer has sufficient mechanical strength to maintain stress in said strained silicon body after said first aperture is formed.

[c5] A method according to claim 4, further comprising a

step of:

removing said pair of temporary dielectric spacers after said step of forming said electrode layer of silicon in said first aperture; and

forming said transition doped areas by implanting dopants in said electrode layer of silicon.

[c6] A method according to claim 5, further comprising a step of:

removing SiGe alloy from said support layer below said S/D aperture, thereby extending said first S/D aperture vertically downward to form a second S/D aperture; and forming said electrode layer of silicon in said second aperture with an electrode layer thickness greater than said strained silicon layer thickness.

[c7] A method according to claim 1, further comprising a step of:

removing SiGe alloy from said support layer below said S/D aperture, thereby extending said first S/D aperture vertically downward to form a second S/D aperture; and forming said electrode layer of silicon in said second aperture with an electrode layer thickness greater than said strained silicon layer thickness.

[c8] A method according to claim 7, further comprising a step of:

after said step of forming said transition doped areas, forming a pair of spacers between said gate electrode and source and drain areas in said electrode layer of silicon on opposite sides of said gate electrode and forming source and drain electrodes in said source and drain areas.

[c9] A method according to claim 8, in which said temporary spacers have a thickness abutting said strained silicon layer such that said buffer portion of strained silicon in said strained silicon layer has sufficient mechanical strength to maintain stress in said strained silicon body after said first aperture is formed.

[c10] A method according to claim 1, in which said electrode layer of silicon is formed in said second aperture up to at least the level of said gate dielectric.

[c11] A method according to claim 10, in which said temporary spacers have a thickness abutting said strained silicon layer such that said buffer portion of strained silicon in said strained silicon layer has sufficient mechanical strength to maintain stress in said strained silicon body after said first aperture is formed.

[c12] A method according to claim 11, further comprising a step of:

removing said pair of temporary dielectric spacers after said step of forming said electrode layer of silicon in said first aperture; and

forming said transition doped areas by implanting dopants in said electrode layer of silicon.

[c13] A method according to claim 12, further comprising a step of:

removing SiGe alloy from said support layer below said S/D aperture, thereby extending said first S/D aperture vertically downward to form a second S/D aperture; and forming said electrode layer of silicon in said second aperture with an electrode layer thickness greater than said strained silicon layer thickness.

[c14] An NFET having a strained silicon transistor body in a layer of strained silicon, having a strained silicon layer thickness, disposed on a support layer of SiGe alloy, comprising:

a gate dielectric over said strained silicon transistor body;

a gate electrode over said gate dielectric; and

a pair of transistor electrodes in electrode areas on opposite sides of said gate electrode, separated from said gate electrode by an extension area, in which;

said transistor electrodes are formed in an electrode layer of silicon outside said transistor body, separated

from said transistor body by a buffer portion of strained silicon in said strained silicon layer and making mechanical and electrical contact with said transistor body.

[c15] An NFET according to claim 14, in which said electrode layer of silicon extends downward past a lower surface of said transistor body, thereby increasing an electrode cross section of said transistor electrodes.

[c16] An NFET according to claim 14, in which said electrode layer of silicon is formed by epitaxial growth on an exposed surface of said support layer of SiGe alloy.

[c17] An NFET according to claim 14, in which said electrode layer of silicon extends upward above a top surface of said transistor body.

[c18] An integrated circuit comprising a set of PFET transistors and a set of NFET transistors connected to form an electrical circuit, in which at least one NFET has
a strained silicon layer thickness, disposed on a support layer of SiGe alloy;
a gate dielectric over said strained silicon transistor body;
a gate electrode over said gate dielectric; and
a pair of transistor electrodes in electrode areas on opposite sides of said gate electrode, separated from said

gate electrode by an extension area, in which;
said transistor electrodes are formed in an electrode layer of silicon outside said transistor body, separated from said transistor body by a buffer portion of strained silicon in said strained silicon layer and making mechanical and electrical contact with said transistor body.

[c19] An integrated circuit according to claim 18, in which said electrode layer of silicon is formed by epitaxial growth on an exposed surface of said support layer of SiGe alloy.

[c20] An integrated circuit according to claim 18, in which said electrode layer of silicon extends upward above a top surface of said transistor body.